

PUBLICATIONS

Synchronous Equipment timing source Module

Features:

- ? *Stratum 3 ,Stratum 4 clock quality*
- ? *Meeting the GR1244 GR 253 requirements.*
- ? *Supporting 24hr holdover mode*
- ? *Four control bit interface.*
- ? *Small footprint*
- ? *Available now*
- ? *Low cost solution for complex problem*

There are very stringent Bellcore and ITU specifications regarding clocking in networks. The design of network clocks is not a trivial task, requiring temperature compensated voltage controlled oscillator-based phase locked loop designs. The clocks are required to meet wander and jitter standards. Upon failure of both main and standby clocks, the standard requires that the holdover clock be maintained with a very high level of accuracy. For example, Stratum level 3 clocking systems are required to have less than 255 slips in the first 24 hours of loss of network clock. As an example the TDM Cross Connect must use the Stratum 3 clock to align and synchronize all TDM frames.

Our testing indicates that powerxlogic stratum-3 TSG does provide a clock whose wander generation is under the criteria of GR-1244 and GR-253. Result show the wander generation we observed. B.T.W., result shows the jitter generation we observed.

Wander Generation

Wander generation is one of the most important characteristics of a stratum-3 or a higher-level TSG (timing signal generator). It is measured by locking on an input reference that is free of wander and jitter. Usually, engineers use TDEV and MTIE to present the quantity of wander.

We powered up our TSG more than 10 minutes before any testing. This process is to make sure that all the clocks/oscillators are warmed up to a stable state. The oven controlled crystal oscillators take time to achieve its targeted temperature.

In powerxlogic lab, we use HP DS345 Synthesized Function Generator to generate our input 19.44 MHz reference. The DS345 is linked to a LORAN-C stratum-i reference in order to create a clear signal.

Phase Hit

In powerxlogic lab, a sudden 1,000 ns phase hit (transient) was applied to the input target reference clock to simulate the most extreme phase hit requirement on GR- 1244. In this section, we are going to show that powerxlogic TSG can meet the general requirements.

The frequency of this input reference can be 19.44MHz, 77.76 MHZ . It was also modulated with 10 Hz 200 ns span noise to simply simulate the noisy environment.

By our design, the output phase transient phenomena caused by the input phase hit will not exceed 60 seconds.

GR-1244 Section 5.6 states that with an input phase transient of up to 1000 ns, the output phase transient shall occur with 64 seconds for a stratum-3 clock. After 64 seconds, the MTIE and TDEV of

the output clock shall satisfy the output wander generation requirements. Result show the wander measured 60 seconds after the phase hit. Both the MTIE and TDEV values satisfy the wander generation requirements of an output clock on GR-1244 and GR-253.

Reference Rearrangement

GR- 1244 Section 5.6 states that the timing reference switching shall not cause output phase transient occur more than 64 seconds for a stratum 3 clock. After 64 seconds, the MTIE and TDEV of the output clock shall satisfy the output wander generation requirements. However, the design goal of powerxlogic TSG is to provide even a *hit-less* timing reference switching. Result shows the wander during the reference rearrangement process. Be ware that the measurement was started 20 seconds before the timing reference switching, not 60 seconds after it. Both the MTIE and TDEV values satisfy the wander generation requirements of an output clock on GR-1244 and GR-253. This means that the timing reference switching does not even impact the output clock of powerxlogic TSG. The TSG just quickly re-establish a new phase error relation between its output clock and the new reference clock. This is what we

Hit less reference switching

Both two input references have same frequency, 19.44MHz. But, both of them were also modulated with 10 Hz 200 ns span noise to simply simulate the noisy environment. There is a 2.93 ns phase error between those two references.

The maximum settling time, the time to achieve lock after a new reference becoming active, is 100 seconds for a stratum3 clock defined on GR-1244. If the frequency of the new reference is different to the current frequency of its output clock, the output phase change occurs during the pull-in process. The maximum phase changes during pull-in process are also defined on GR-1244. In powerxlogic lab, we test this scenario by switching between two reference clocks with up to 20 ppm

frequency offset.

Result shows the wander of output clock during the pull-in process. The measurement was started at the same time the reference switching happened. We can see that the phase change in this extreme case is 60 ?sec. The general requirement allows up to 450 ?sec under the same situation.

Then, we move to observe the behavior of the output reference after the maximum settling time, 100 seconds for a stratum 3 clock. Figure 10 and Figure 11 display the wander of the output reference. The measurement was started 100 seconds after the reference-offset switching. We can see that both the TDEV and MTIE do satisfy the requirements of wander generation.

